IN THE CLAIMS:

The claims are to be amended as noted. Please note that all claims currently pending and under consideration in the referenced application are shown below, in clean form, for clarity. Please enter these claims as amended. Also attached is a version with markings to show changes made to the claims.

1. (Amended twice) A method for making a metallization structure for a semiconductor device, comprising:
forming a substantially planar first dielectric layer on a substrate;
forming at least one metal containing layer over the first dielectric layer;
forming a single conducting layer over the at least one metal containing layer;
forming a second dielectric layer over the single conducting layer;
removing aligned portions of the second dielectric layer, single conducting layer, and at least one metal containing layer to form a multilayer structure; and
forming metal spacers on sidewalls of the multilayer structure, said metal spacers being substantially the same height as said multilayer structure.

2. (Previously Amended) The method of claim 1, wherein said forming the first dielectric layer comprises forming a silicon oxide or BPSG layer.

3. (Amended twice) The method of claim 2, wherein said forming the at least one metal containing layer comprises forming the at least one metal containing layer of Ti, Ta, W, Co or Mo or an alloy or a compound of any thereof, including TaN or TiN.

4. (Amended three times) The method of claim 3, further comprising forming a second metal containing layer between a first metal containing layer of said at least one metal containing layer and the substrate, said second metal containing layer comprising TiN, TiW, WN, or TaN.

5. (Amended twice) The method of claim 1, wherein said forming the at least one metal containing layer comprises forming the at least one metal containing layer of titanium or titanium nitride.

6. (Amended) The method of claim 1, wherein the at least one metal containing layer is a single metal containing layer and further comprising forming the single metal containing layer of titanium or titanium nitride.

7. (Amended twice) The method of claim 1, wherein said forming the single conducting layer comprises forming the single conducting layer from at least one of aluminum and copper.

8. (Amended twice) The method of claim 7, wherein said forming the single conducting layer comprises forming the single conducting layer of an aluminum-copper alloy.

9. (Previously Amended) The method of claim 1, wherein said forming the metal spacers comprises forming at least one layer of Ti, Ta, W, Co or Mo, or alloys thereof or compounds thereof, including TaN and TiN.

10. (Previously Amended) The method of claim 9, wherein said forming the metal spacers comprises forming the metal spacers of titanium or titanium nitride.

11. (Amended twice) The method of claim 1, wherein said forming a second dielectric layer comprises forming the second dielectric layer on the single conducting layer to have sidewalls aligned with sidewalls of the single conducting layer, and forming the metal spacers to extend along the sidewalls of the second dielectric layer.

12. (Previously Amended) The method of claim 11, further comprising forming the second dielectric layer of a low dielectric constant material.

13. (Previously Amended) The method of claim 12, further comprising forming the second dielectric layer of a fluorine-doped silicon oxide.

14. (Amended) The method of claim 1, further comprising forming the at least one metal containing layer and the metal spacers of a same metal.

15. (Amended twice) The method of claim 1, wherein said forming the at least one metal layer containing comprises forming the at least one metal containing layer by vapor deposition.

16. (Amended three times) The method of claim 1, wherein said forming the at least one metal containing layer comprises forming the at least one metal containing layer by CVD, PVD or PECVD.

17. (Amended twice) The method of claim 1, wherein said forming the single conducting layer comprises forming the single conducting layer by vapor deposition.

18. (Amended) The method of claim 17, further comprising forming the single conducting layer by CVD, PVD or PECVD.

19. (Previously Amended) The method of claim 1, wherein said forming the metal spacers comprises forming the metal spacers by vapor deposition and directional etching.

20. (Reiterated) The method of claim 19, further comprising effecting the vapor deposition as CVD, PVD or PECVD.

21. (Amended twice) The method of claim 1, wherein removing aligned portions of the second dielectric layer, single conducting layer, and at least one metal containing layer to form the multilayer structure is effected by patterning and etching the second dielectric layer, the single conducting layer, and the at least one metal containing layer.

22. (Previously twice amended) The method of claim 1, wherein said forming the metal spacers comprises forming a metal spacer layer over the multilayer structure and first dielectric layer and removing portions thereof overlying the first and second dielectric layers.

23. (Previously twice amended) The method of claim 22, wherein said forming the metal spacers comprises forming the metal spacer layer over the multilayer structure and first dielectric layer by a conformal deposition process.

24. (Previously Amended) The method of claim 23, wherein portions of the metal spacer layer over the multilayer structure and first dielectric layer are removed by etching.

25. (Amended) The method of claim 1, further comprising removing any remaining portion of the second dielectric layer and upper portions of the metal spacers laterally adjacent thereto.

26. (Previously Amended) The method of claim 25, further comprising removing any remaining portion of the second dielectric layer and upper portions of the metal spacers by etching.

72. (Amended) A method for constructing a metallization structure for a semiconductor device, comprising:

providing a substrate having a first dielectric layer underlying at least one metal containing layer;

creating a single conducting layer over the at least one metal containing layer;

removing aligned portions of the single conducting layer and at least one metal containing layer to form a multilayer structure; and

flanking at least one surface of the multilayer structure with a metal spacer, said metal spacer being substantially the same height as said multilayer structure.

73. (Amended) The method of claim 72, further comprising forming a second dielectric layer over said single conducting layer.

74. (Reiterated) The method of claim 73, wherein said removing further comprises removing aligned portions of said second dielectric layer to form said multilayered structure.

75. (Reiterated) The method of claim 73, wherein said flanking at least one surface of the multilayer structure with a metal spacer comprises forming a metal spacer layer on said second dielectric layer.

76. (Reiterated) The method of claim 75, further comprising removing any remaining portion of the second dielectric layer and upper portions of the metal spacer layer laterally adjacent thereto.

77. (Reiterated) The method of claim 76, wherein said removing any remaining portion is effected by etching.

78. (Amended) The method of claim 72, wherein said providing a substrate having a first dielectric layer comprises forming said first dielectric layer of a silicon oxide or BPSG layer.

79. (Amended) The method of claim 72, wherein said providing a substrate having a first dielectric layer underlying at least one metal containing layer comprises forming the at least one metal containing layer of Ti, Ta, W, Co or Mo or an alloy or a compound of any thereof, including TaN or TiN.

80. (Amended) The method of claim 79, wherein said forming the at least one metal containing layer comprises forming the at least one metal containing layer of titanium or titanium nitride.

81. (Amended) The method of claim 72, further comprising forming a second metal containing layer between a first metal containing layer of the at least one metal containing layer and the substrate, said second metal containing layer comprising TiN, TiW, WN, or TaN.

82. (Amended) The method of claim 72, wherein the at least one metal containing layer is a single metal containing layer and further comprising forming the single metal containing layer of titanium or titanium nitride.

83. (Amended) The method of claim 72, wherein said creating a single conducting layer comprises forming the single conducting layer from at least one of aluminum and copper.

84. (Amended) The method of claim 72, wherein said creating a single conducting layer comprises creating the single conducting layer of an aluminum-copper alloy.

85. (Reiterated) The method of claim 72, wherein said flanking comprises forming the metal spacer of at least one layer of Ti, Ta, W, Co or Mo, or alloys thereof or compounds thereof, including TaN and TiN.

86. (Reiterated) The method of claim 85, wherein said forming the metal spacer comprises forming the metal spacers of titanium or titanium nitride.

87. (Amended) The method of claim 72, wherein said flanking at least one surface comprises forming said metal spacer on sidewalls of said multilayer structure.

88. (Reiterated) The method of claim 72, wherein said flanking at least one surface comprises forming said metal spacer on a top surface of said multilayer structure.

89. (Amended) The method of claim 72, further comprising forming a second dielectric layer on the single conducting layer to have sidewalls aligned with the conductive layer sidewalls, and forming the metal spacer to extend along the sidewalls of the second dielectric layer.

90. (Reiterated) The method of claim 89, wherein said forming the second dielectric layer comprises forming the second dielectric layer of a low dielectric constant material.

91. (Reiterated) The method of claim 90, wherein said forming the second dielectric layer comprises forming the second dielectric layer of a fluorine-doped silicon oxide.

92. (Amended) The method of claim 72, further comprising forming the at least one metal containing layer and the metal spacer of a same metal.

93. (Amended) The method of claim 72, wherein said providing a substrate having a first dielectric layer underlying at least one metal containing layer comprises forming the at least one metal containing layer by vapor deposition.

94. (Amended) The method of claim 93, wherein said forming the at least one metal containing layer by vapor deposition comprises forming the at least one metal containing layer by CVD, PVD or PECVD.

95. (Amended) The method of claim 72, wherein said creating a single conducting layer comprises forming the conducting layer by vapor deposition.

96. (Amended) The method of claim 95, wherein said forming the single conducting layer by vapor deposition comprises forming the single conducting layer by CVD, PVD or PECVD.

97. (Reiterated) The method of claim 72, wherein said flanking comprises forming the metal spacer by vapor deposition and directional etching.

98. (Reiterated) The method of claim 97, further comprising effecting the vapor deposition as CVD, PVD or PECVD.

99. (Amended) The method of claim 72, wherein removing aligned portions of the single conducting layer and at least one metal containing layer to form a multilayer structure is effected by patterning and etching the single conducting layer and the at least one metal containing layer.

100. (Reiterated) The method of claim 72, wherein said flanking comprises forming the metal spacer by forming a metal spacer layer over the multilayer structure and first dielectric layer and removing portions thereof overlying the first dielectric layer and a top portion of said multilayer structure.

101. (Amended) The method of claim 100, wherein said forming the metal spacer layer over the multilayer structure and first dielectric layer comprises forming the metal containing layer by a conformal deposition process.

102. (Reiterated) The method of claim 101, wherein said removing portions of the metal spacer layer is effected by etching.

103. (New) A method for making a metallization structure for a semiconductor device, comprising:

forming a substantially planar first dielectric layer on a substrate;

forming at least one metal containing layer over the first dielectric layer;

forming a conducting layer over the at least one metal containing layer;

forming a second dielectric layer over the conducting layer;

removing aligned portions of the second dielectric layer, conducting layer, and at least one metal containing layer to form a multilayer structure;

forming metal spacers on sidewalls of the multilayer structure; and

removing any remaining portion of the second dielectric layer and upper portions of the metal spacers laterally adjacent thereto.

104. (New) The method of claim 103, wherein said removing any remaining portion is effected by etching.

105. (New) A method for constructing a metallization structure for a semiconductor device, comprising:

providing a substrate having a first dielectric layer underlying at least one metal containing layer;

creating a conducting layer over the at least one metal containing layer;

removing aligned portions of the conducting layer and at least one metal containing layer to form a multilayer structure;

flanking at least one surface of the multilayer structure with a metal spacer; and

removing any remaining portion of the second dielectric layer and upper portions of the metal spacer layer laterally adjacent thereto.

106. (New) The method of claim 105, wherein said removing any remaining portion is effected by etching.